SAMSUNG ELECTRONICS

Evaluation Board Manual

S3F401F

16/32-BIT RISC MICROPROCESSOR

Dec, 2007

REV 1.00

Table of Contents

Chapter 1 Evaluation Board Manual

1 EVALUATION BOARD MANUAL

1. OVERVIEW

S3F401F EVB (Evaluation Board) is a compact platform that is suitable for code development of SAMSUNG's S3F401F 16-/32-bit RISC microcontroller for an inverter motor and general purpose application.

EVB is consists of several blocks, which can make operate the function of S3F401F. Those functions are from the followings:

- A 16-/32-bit RISC CPU Core, ARM7TDMI-S
- A built-in 256Kbyte NOR-Flash memory
- An internal 20KB SRAM for stack, data, or code
- An interrupt controller, supporting vectored interrupt
- 6xch 16-bit timers with capture and PWM function
- 1xch 8-bit basic timer & 3-bit watch-dog timer
- Three programmable I/O port groups
- 2xch Inverter motor controller
- 2xch 16-bit Encoder counter
- 15xch 12-bit ADC
- 2xch UART
- 2xch SSP

If you need more detail information about S3F401F, meet the samsung web site.
http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=223

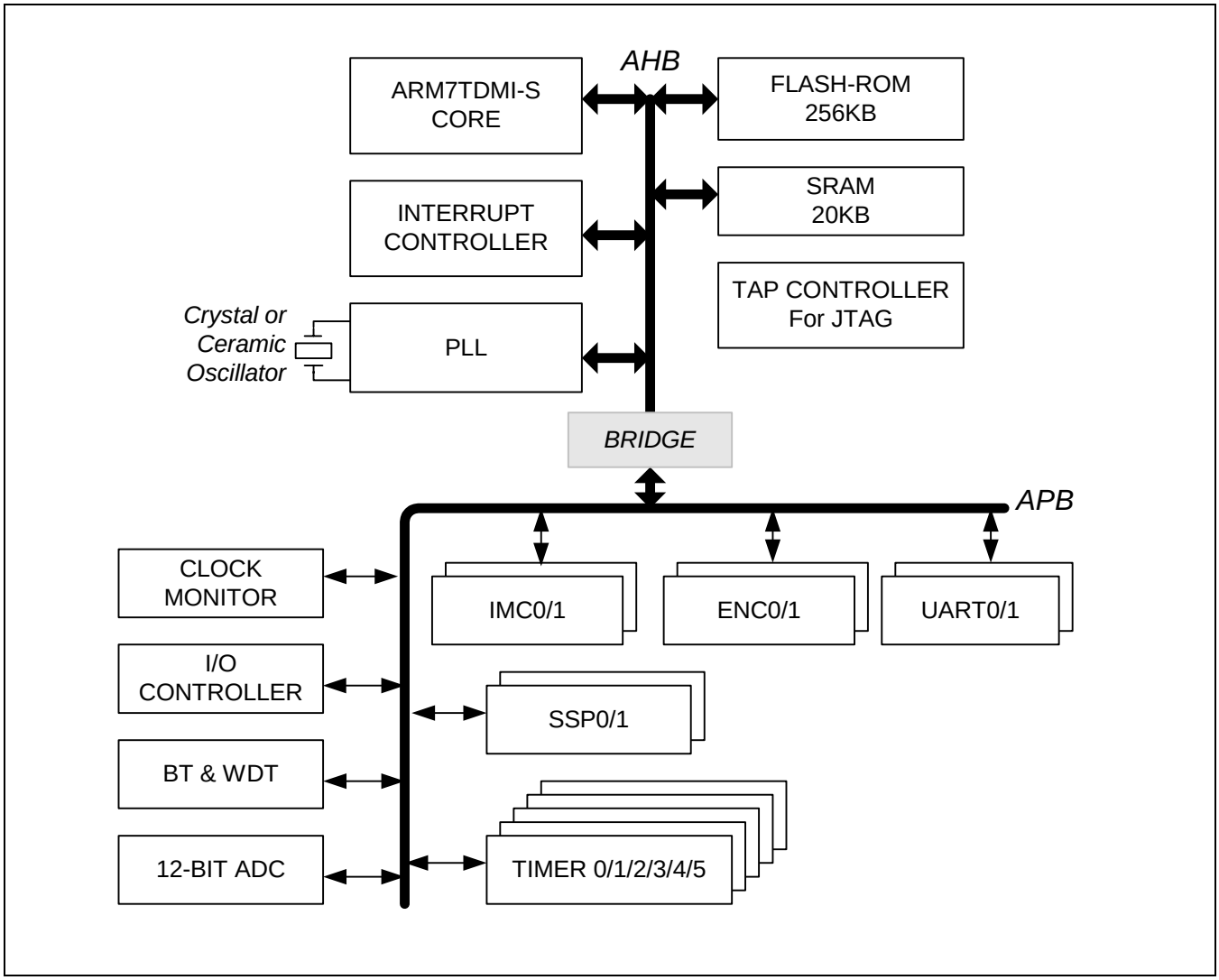


Figure 1. S3F401F Block Diagram

1.1 FEATURES

Micro-Controller	S3F401F, ARM7TDMIS, 16/32-bit RISC Microcontroller
Board Power Source	External DC 7~12V
	Adjustable voltage regulator out is 3.2V
Board Master Power Switch	SW6
UART	Support to protocol for RS-232
	Physical interface circuit connected to standard PC through DB9(female)
	Interface driver IC MAX3221
Synchronous Serial Port	Provide SSP, SPI serial communication with external devices (master or slave)
	SSP serial EEPROM (8K * 8bit): X25650
	SSP serial EEPROM (4K * 16bit): 64LC40S
LED	IO Port output control display
JTAG Connection	20Way JTAG connector (Multi-ICE Interface, Trace 32 etc.)

1.2 SYSTEM REQUIREMENTS

This section describes the hardware and software system requirements.

Software Requirements	ARM Compiler SW
	ARM Debugger SW
Hardware Requirements	S3F401F EVB Board Set
	Power Supply DC 7~12V (Recommend Default 12V)
	Debugger (Multi-ICE or Trace 32 etc.)
	PC(Pentium, 32MB RAM for Windows 95, or 64MB RAM for Windows NT)
	COM Port for serial communication
	Parallel Port (If using Multi-ICE)

1.3 BOARD COMPONENTS

The board consists of the followings.

S3F401F Micro-controller
64LC40S and X25650 as a serial EEPROM for SSP
2 x DSUB Connector for RS-232
2 x Header groups for IMC function
1 x Buzzer
6 x Switches: IRQ x 2, Power, Reset
4 x LED: Power x1, IO Port output x 3
A regulator to generate 3.3V
4MHz Crystal as a master system clock source
Switches for ADC input capacitor selection
7-segment (4-digit) display circuit
A standard 20-pin JTAG interface connector
Dual-line header pins for a port level or signal
53 x Jumpers for function setting control
15 x TP (Test Pole) to check specific pins relating to the digital, analog, PLL power and clock

2. CONFIGURATION

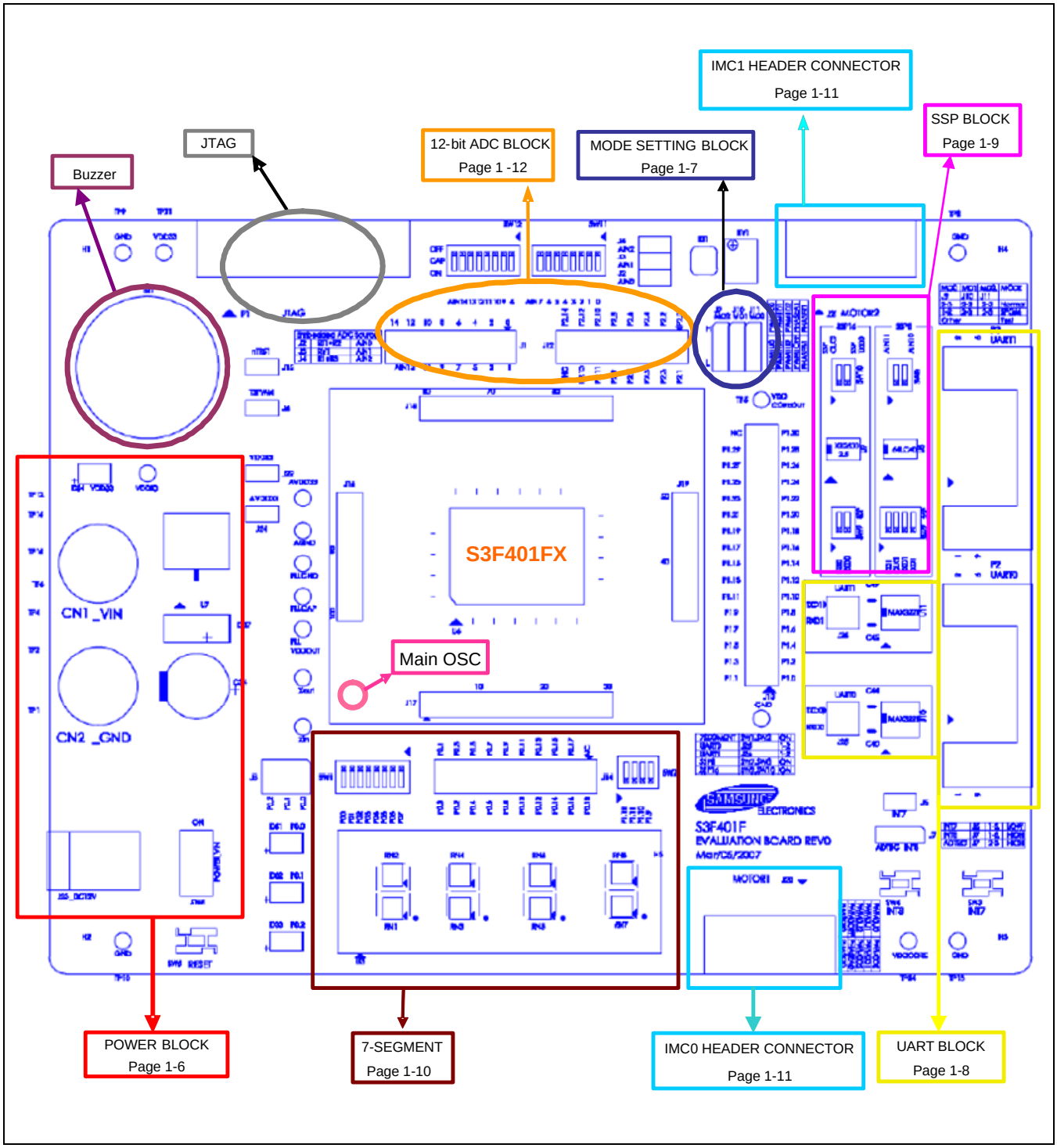
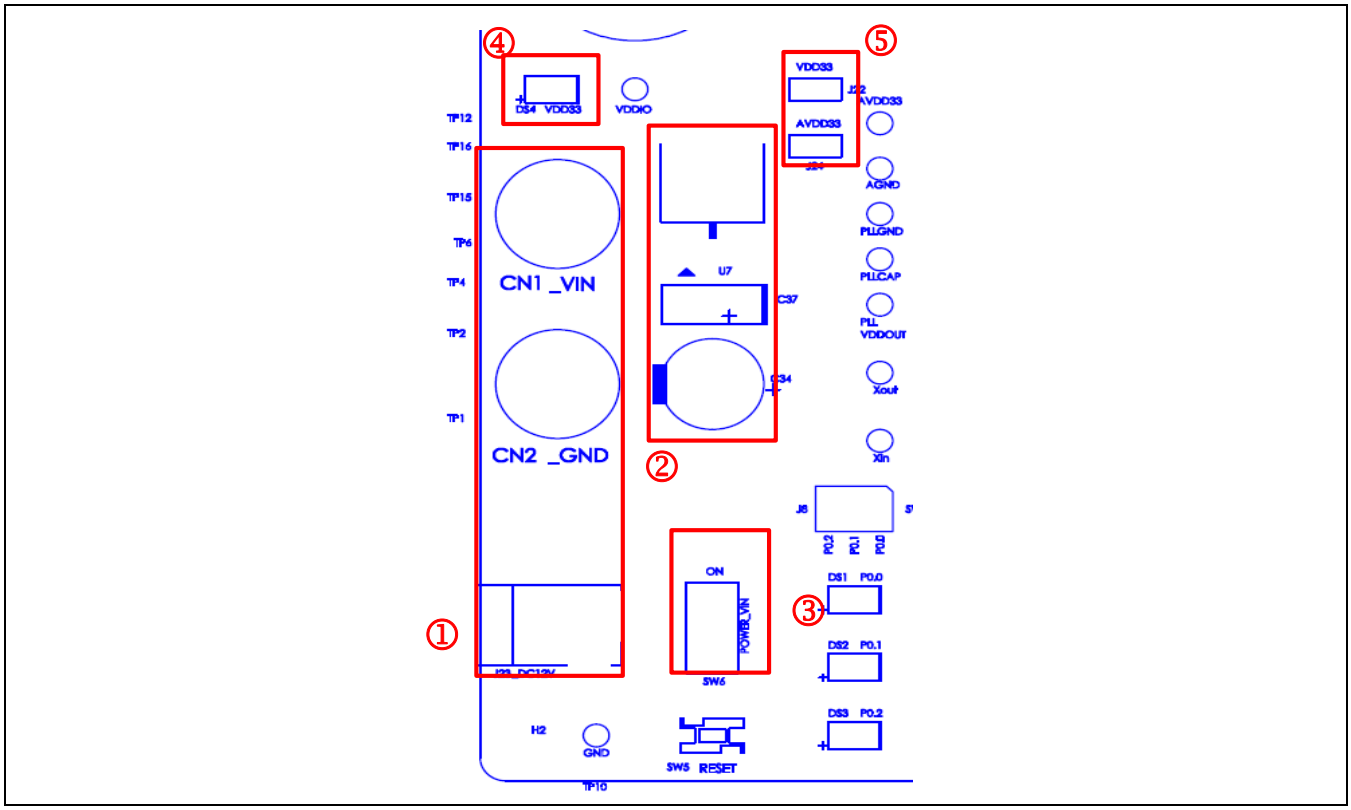


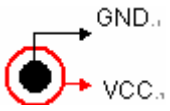
Figure 2. S3F401F Evaluation Board Top-view

2.1 DETAILED BLOCK CONFIGURATIONS

2.1.1 Power Block



① **CN1, CN2, J23:** Power Supply Connector
CN1 **:** VIN
CN2 **:** GND
J23 **:** DC adapter connector



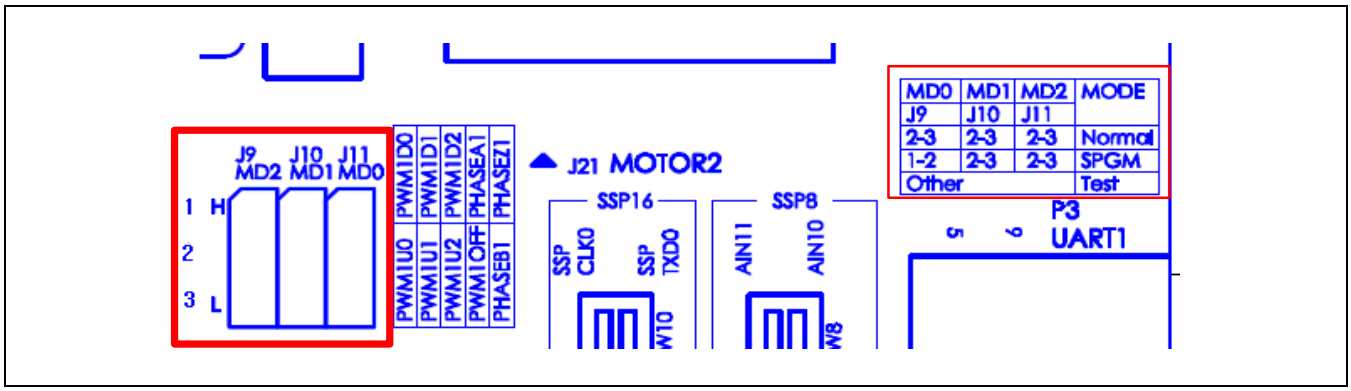
② **U7:** Adjustable Voltage Regulator
3.3V generator → VDD33, VDDCORE, VDDIO

③ **SW6:** Power Switch

④ **DS4:** Power Display LED
VDD33 Power-on status display

⑤ **J22:** Jumper Setting
Selection VDDCORE / VDDIO
1-2 connection: The VDD of each block is connected to VDD33.

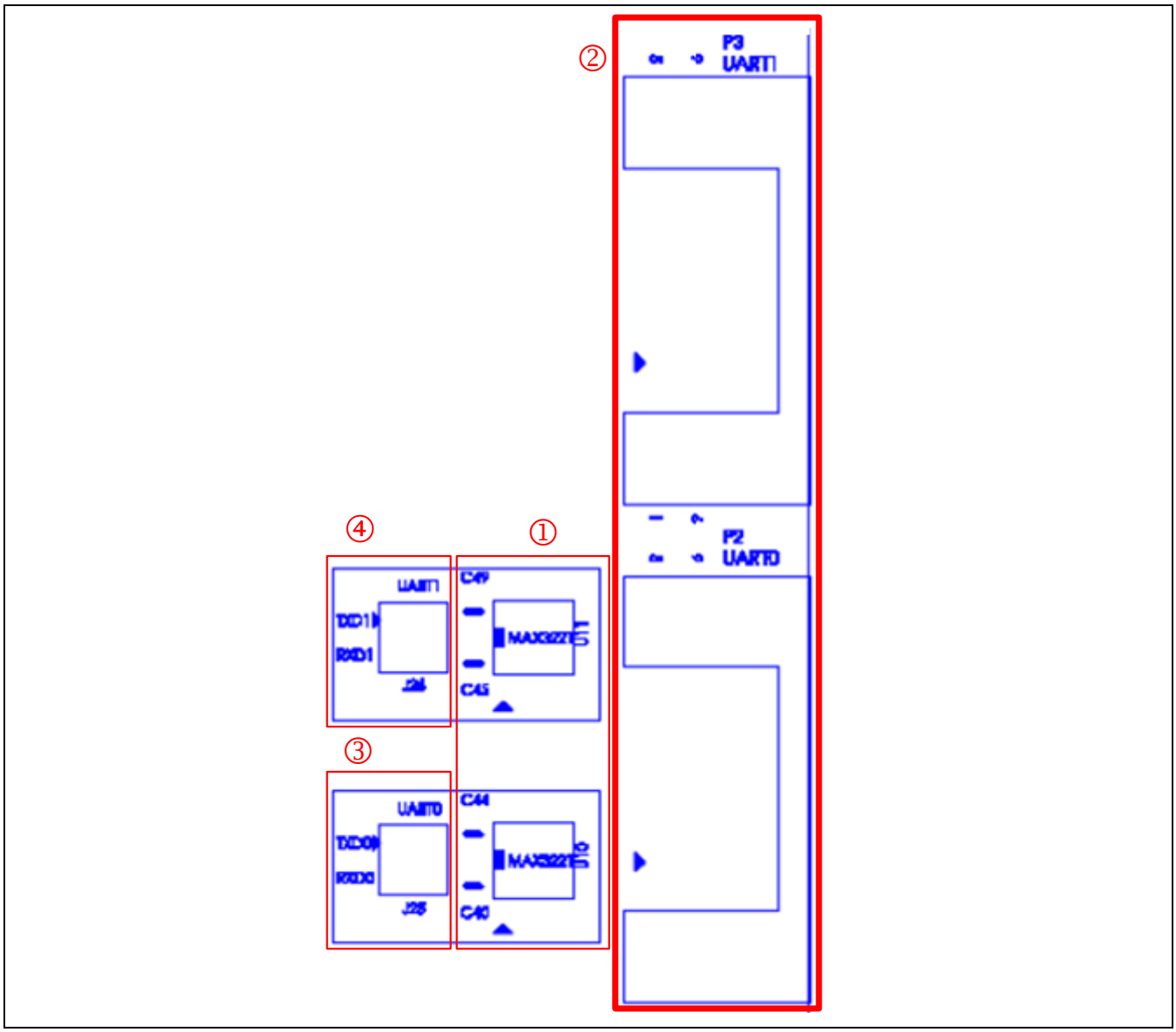
2.1.2 Mode Setting Block



J9 & J10 & J11: Jumper Setting

J9	J10	J11	MD[2:0]
2-3 Connection	2-3 Connection	2-3 Connection	NORMAL
1-2 Connection	2-3 Connection	2-3 Connection	SPGM
Others			Only TEST Mode

2.1.3 UART Block



① **U10, U11:** UART Driver IC

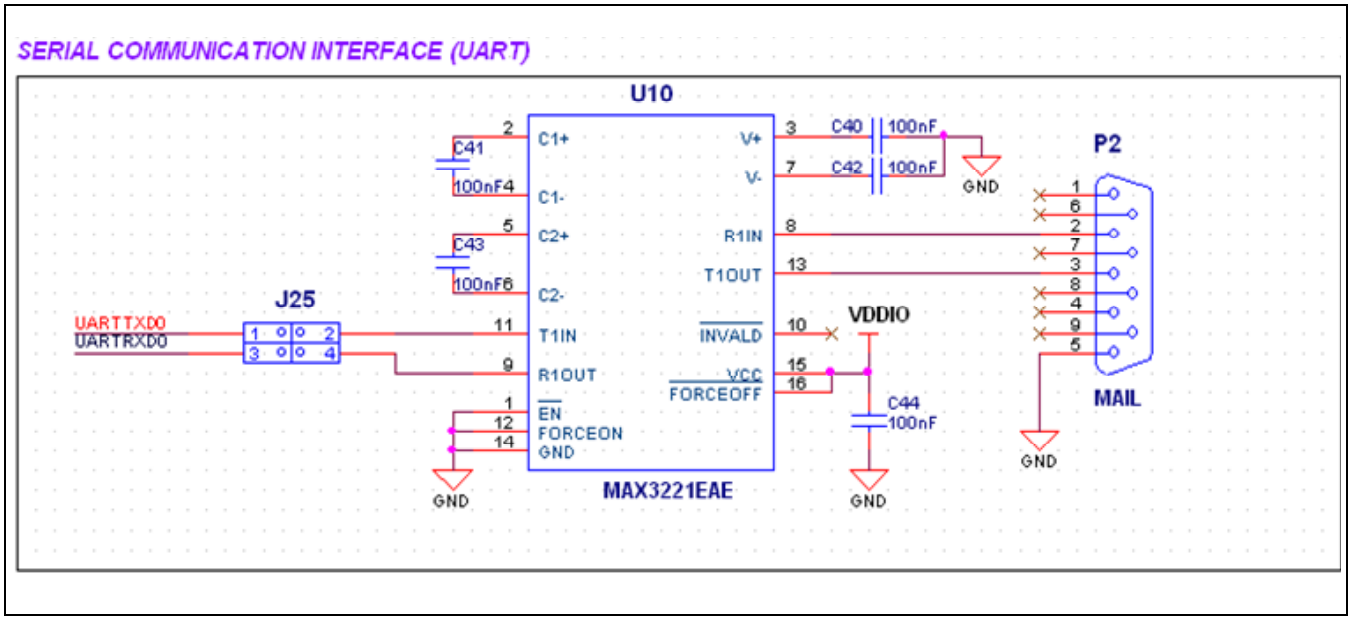
② **P2, P3:** UART Connector

③ **J25** Jumper Setting

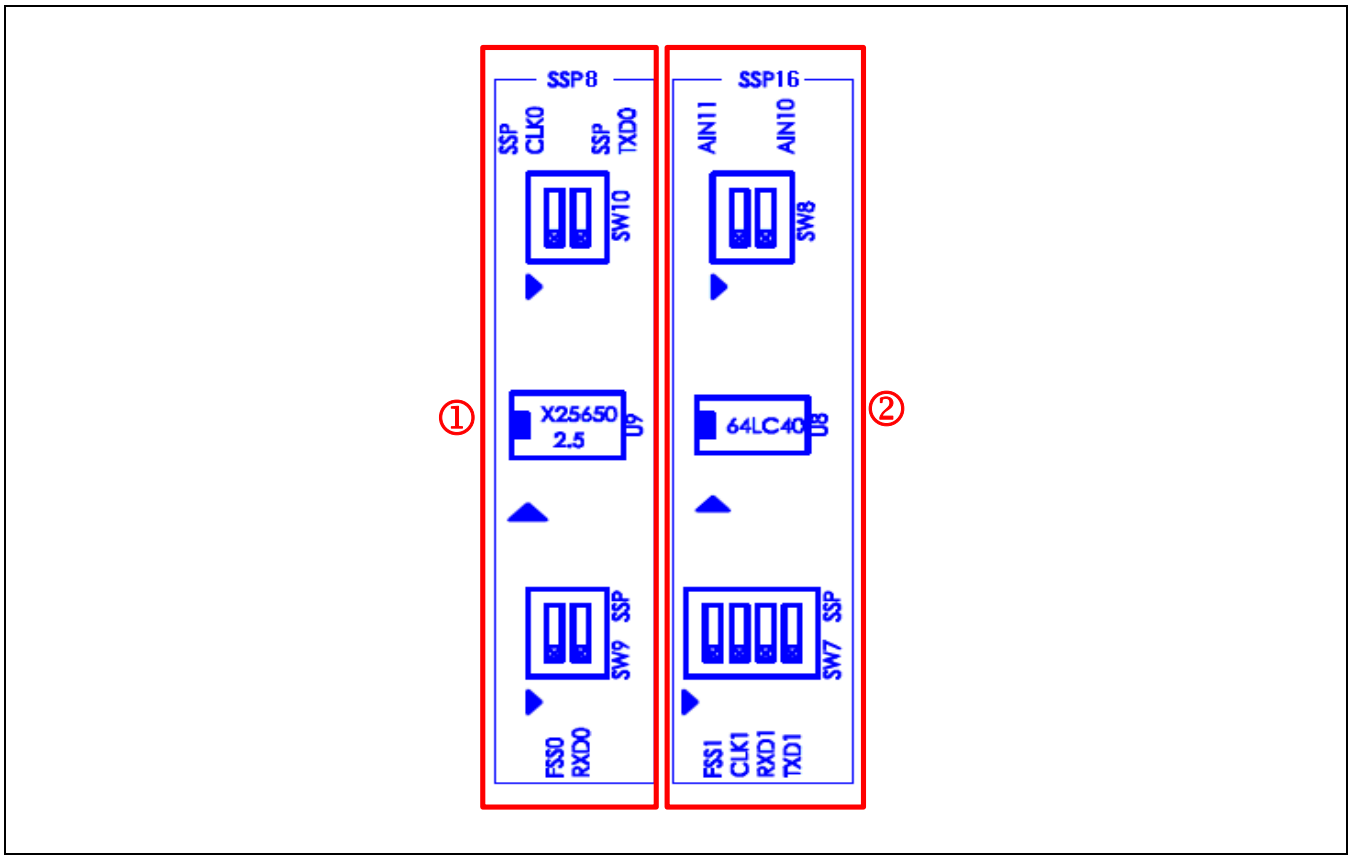
TXD0	UARTTXD0 is connected to T1IN of MAX3221.
RXD0	UARTRXD0 is connected to R1OUT of MAX3221.

④ **J26** Jumper Setting

TXD1	UARTTXD1 is connected to T1IN of MAX3221
RXD1	UARTRXD1 is connected to R1OUT of MAX3221.


SERIAL COMMUNICATION INTERFACE (UART)
U10
C1+
C1-
C2+
C2-
T1IN
R1OUT
EN
FORCEON
GND
V+
V-
R1IN
T1OUT
INVALD
VCC
FORCEOFF
MAX3221EAE
C41
100nF
C43
100nF
C40
100nF
C42
100nF
C44
100nF
GND
VDDIO
J25
UARTTXD0
UARTRXD0
P2
MAIL

2.1.4 SSP Block

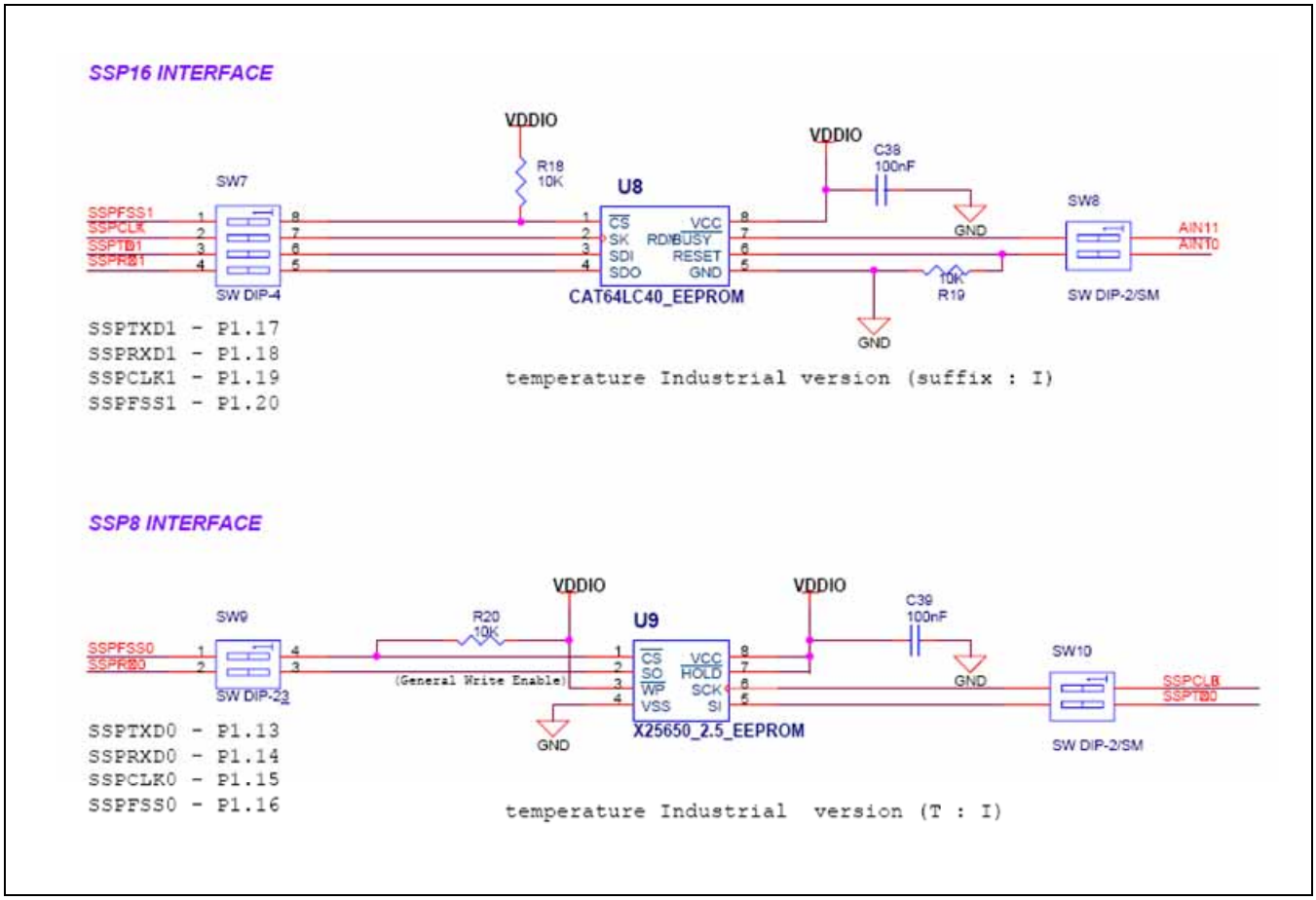


① **U9:** SSP8 serial EEPROM (8K × 8bit)

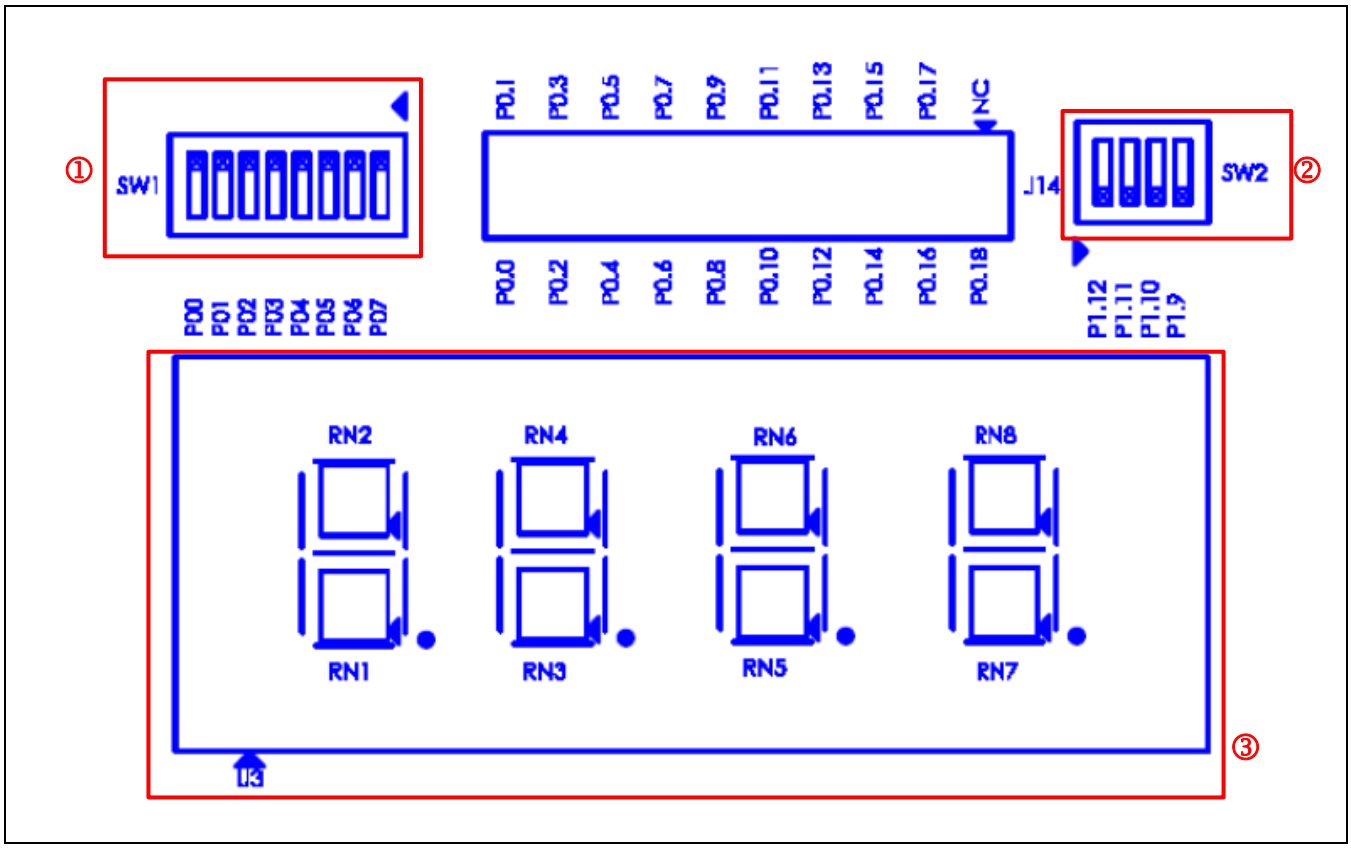
SW9 ON FSS0 is connected to P1.16.
RXD0 is connected to P1.14.
SW10 ON CLK0 is connected to P1.15.
TXD0 is connected to P1.13.

② **U8:** SSP16 serial EEPROM (4K × 16bit)

SW7 ON FSS1 is connected to P1.20.
CLK1 is connected to P1.19.
RXD1 is connected to P1.18.
TXD1 is connected to P1.17.
SW8 ON The RDY/nBUSY pin is connected to P2.11.
The RESET pin is connected to P2.10.


SSP16 INTERFACE
VDDIO
R18
10K
U8
VDDIO
C38
100nF
SW7
SSPFSS1
SSPCLK
SSPTXD1
SSPRXD1
SW DIP-4
CS
SK
SDI
SDO
VCC
RDY/BUSY
RESET
GND
CAT64LC40_EEPROM
GND
SW8
AIN11
AINT0
10K
R19
SW DIP-2/SM
SSPTXD1 - P1.17
SSPRXD1 - P1.18
SSPCLK1 - P1.19
SSPFSS1 - P1.20
temperature Industrial version (suffix : I)
SSP8 INTERFACE
VDDIO
VDDIO
C39
100nF
SW9
R20
10K
U9
SW10
SSPFSS0
SSPRXD0
SW DIP-2
(General Write Enable)
CS
SO
WP
VSS
VCC
HOLD
SCK
SI
GND
X25650_2.5_EEPROM
GND
SSPCLK0
SSPTXD0
SW DIP-2/SM
SSPTXD0 - P1.13
SSPRXD0 - P1.14
SSPCLK0 - P1.15
SSPFSS0 - P1.16
temperature Industrial version (T : I)

2.1.5 7-SEGMENT BLOCK



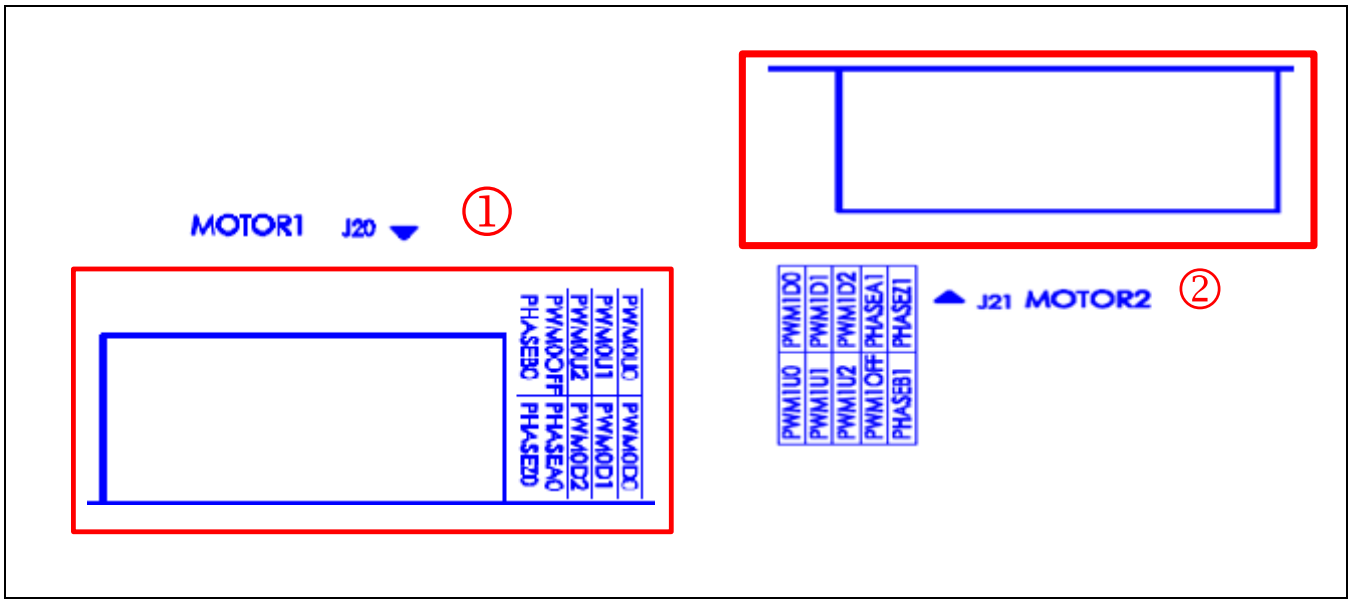
The assignment of 7-segment control pins on the S3F401F-EVB is the same like this.

① **SW1 ON:** This Port (P0.0~P0.7) is connected to each segment of 7-segment.

② **SW2 ON:** This Port (P1.9~P1.12) is connected to latch.

③ **U3:** 7-segment display

2.1.6 IMC BLOCK

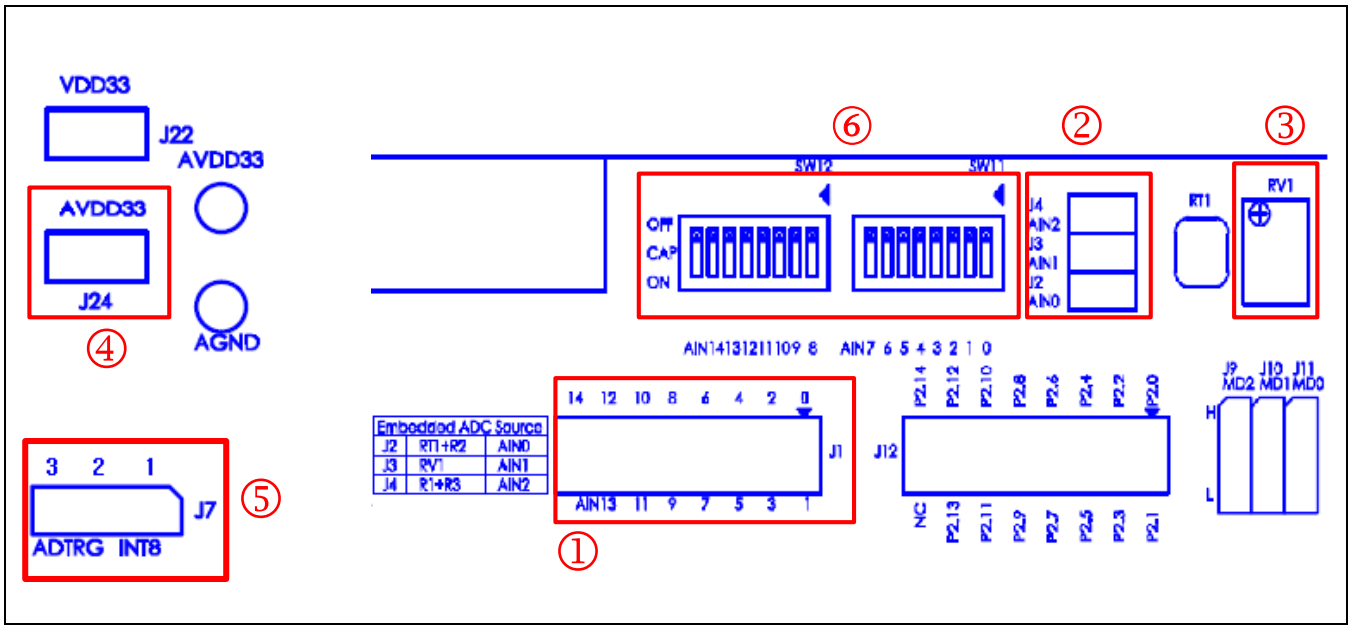


The assignment of IMC pins on the S3F401F-EVB is the same like this.

① **J20:** A header pin group for MOTOR1

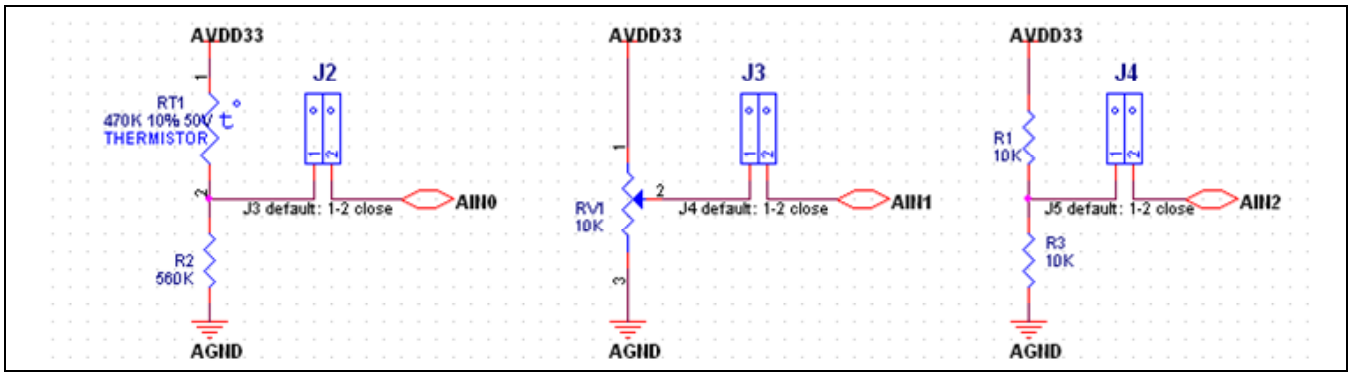
② **J21:** A header pin group for MOTOR2

2.1.7 ADC BLOCK



① **J1:** ADC input connector

② **J2, J3, J4:** J2, J3 and J4 are selected to sample test with AIN0, AIN1 and AIN2



③ **RV1:** Variable Resistor

④ **J24:** ADC Power Source
Close**:** When connecting (short), AVDD is same to VDD33.
Open**:** AVDD is a second (right) pin of J24. So, AVDD should be connected to another power.

⑤ **J7:** 2,3 connection - ADTRG signal is generated by SW4

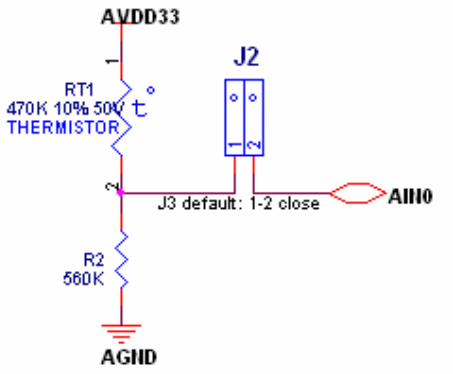
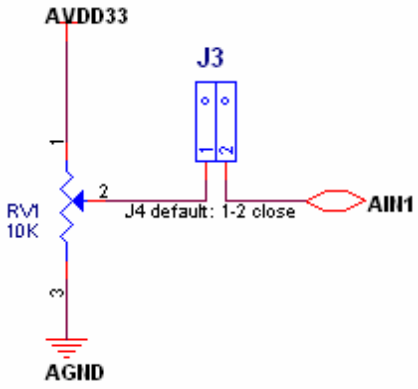
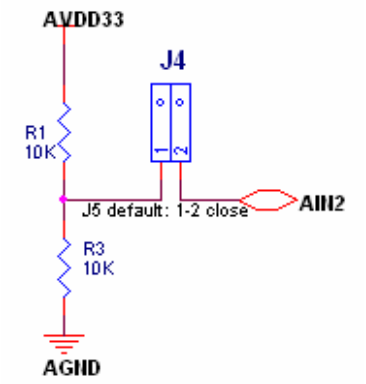
⑥ **SW11, SW12:** Control cap for each ADC input port.

3. TOTAL BLOCKS' UNIT & JUMPER SUMMURY

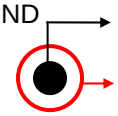
3.1 FUNCTION BLOCKS

Block	Symbols	Description
7-SEGMENT	U3	4Digit Segment
IMC	J20	MOTOR 1
	J21	MOTOR 2
UART	U14	RS-232 transceiver
	P41	RS-232 connector
SSP	U7	SPI8 interface EEPROM (8K × 8bit)
	U8	SPI16 interface EEPROM (4K × 16bit)
	J28	SPI block pin assignment
POWER	U11	3.3V generator regulator
LED	DS1	Red LED
	DS2	Green LED
	DS3	Yellow LED
BUZZER	BZ1	Buzzer

3.2 JUMPER CONNECTION

JP#	Description		Default Setting
J1	ADC block pin assignment	AIN0~AIN14	–
J2	AIN0 input voltage connector		Connect (Short)
J3	AIN1 input voltage connector		Connect (Short)
J4	AIN2 input voltage connector		Connect (Short)
J5	SW3_INPUT	VDDIO connects to INT7	Open
J6	Buzzer connector	T3PWM connects to Buzzer	Connect (Short)
J7	SW4_INPUT	VDDIO connects to INT8	Connect ADTRG
J8	LED signal connector	Port 0.0/0.1/0.2 connect to DS1, DS2, DS3	Connect (Short)

3.2 JUMPER CONNECTION (Continued)

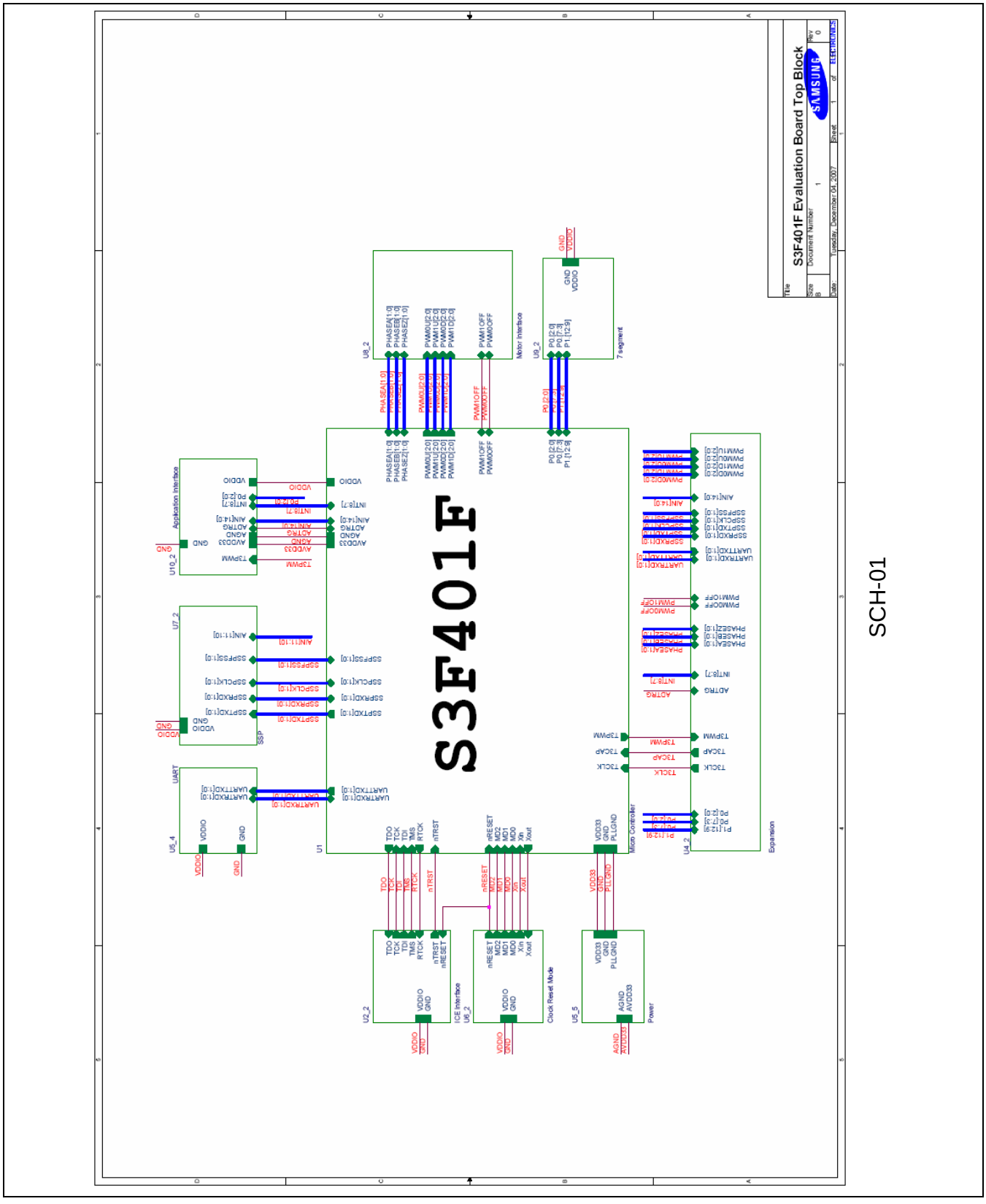
<table>
<tr><th>JP#</th><th colspan="6">Description</th><th>Default Setting</th></tr>
<tr><td>J9
J10
J11</td><td>MODE selection</td><td>J9
2-3
1-2</td><td>J10
2-3
2-3</td><td>J11
2-3
2-3</td><td>MD[1:0]
NORMAL
SPGM</td><td>All 2-3 connect
:Normal Mode</td></tr>
<tr><td>J12</td><td>Port assignment pin</td><td colspan="4">Port 2</td><td>Open</td></tr>
<tr><td>J13</td><td>Port assignment pin</td><td colspan="4">Port 1</td><td>Open</td></tr>
<tr><td>J14</td><td>Port assignment pin</td><td colspan="4">Port 0</td><td>Open</td></tr>
<tr><td>J15</td><td>nTRST</td><td colspan="4">The JTAG connects to nTRST</td><td>Open</td></tr>
<tr><td>J16
J17
J18
J19</td><td>Chip socket connection</td><td colspan="4">Chip socket board is connected with S3F401F-EVB.</td><td>Use the chip socket board</td></tr>
<tr><td>J20</td><td>MOTOR1</td><td colspan="4">IMC0 and ENC0 signal connector</td><td>-</td></tr>
<tr><td>J21</td><td>MOTOR2</td><td colspan="4">IMC1 and ENC1 signal connector</td><td>-</td></tr>
<tr><td>J22</td><td>Generated VDD33 voltage from U11_regulator (3.3V)</td><td colspan="4">3.3V connects to VDD33</td><td>Join 1-2</td></tr>
<tr><td>J23</td><td>DC Power jack (9~18V)</td><td colspan="4">GND
 
VCC</td><td>-</td></tr>
<tr><td>J24</td><td>AVDD</td><td colspan="4">-</td><td>Open</td></tr>
<tr><td>J25
J26</td><td>UART</td><td colspan="4">-</td><td>Open</td></tr>
</table>

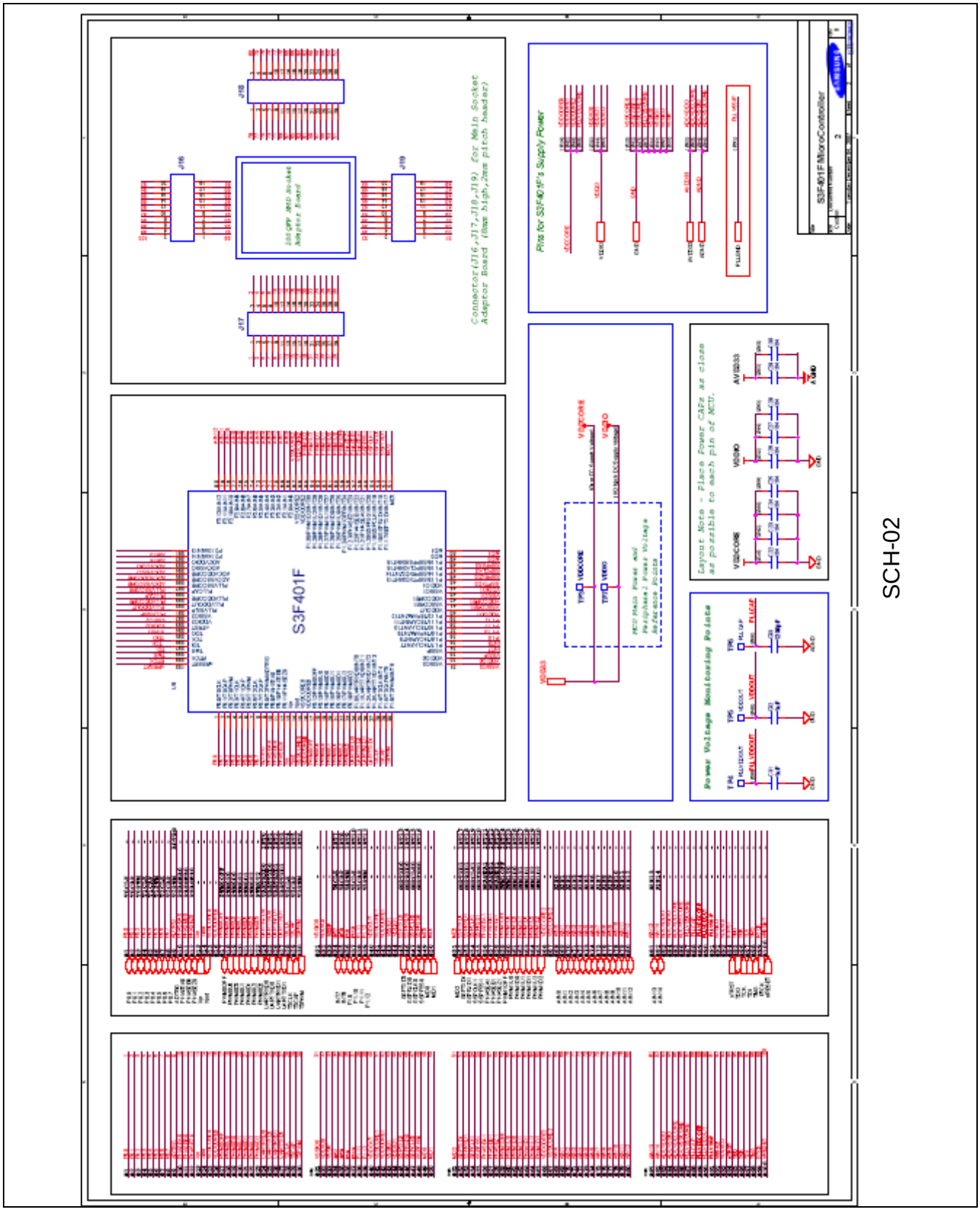
3.3 SWITCHES

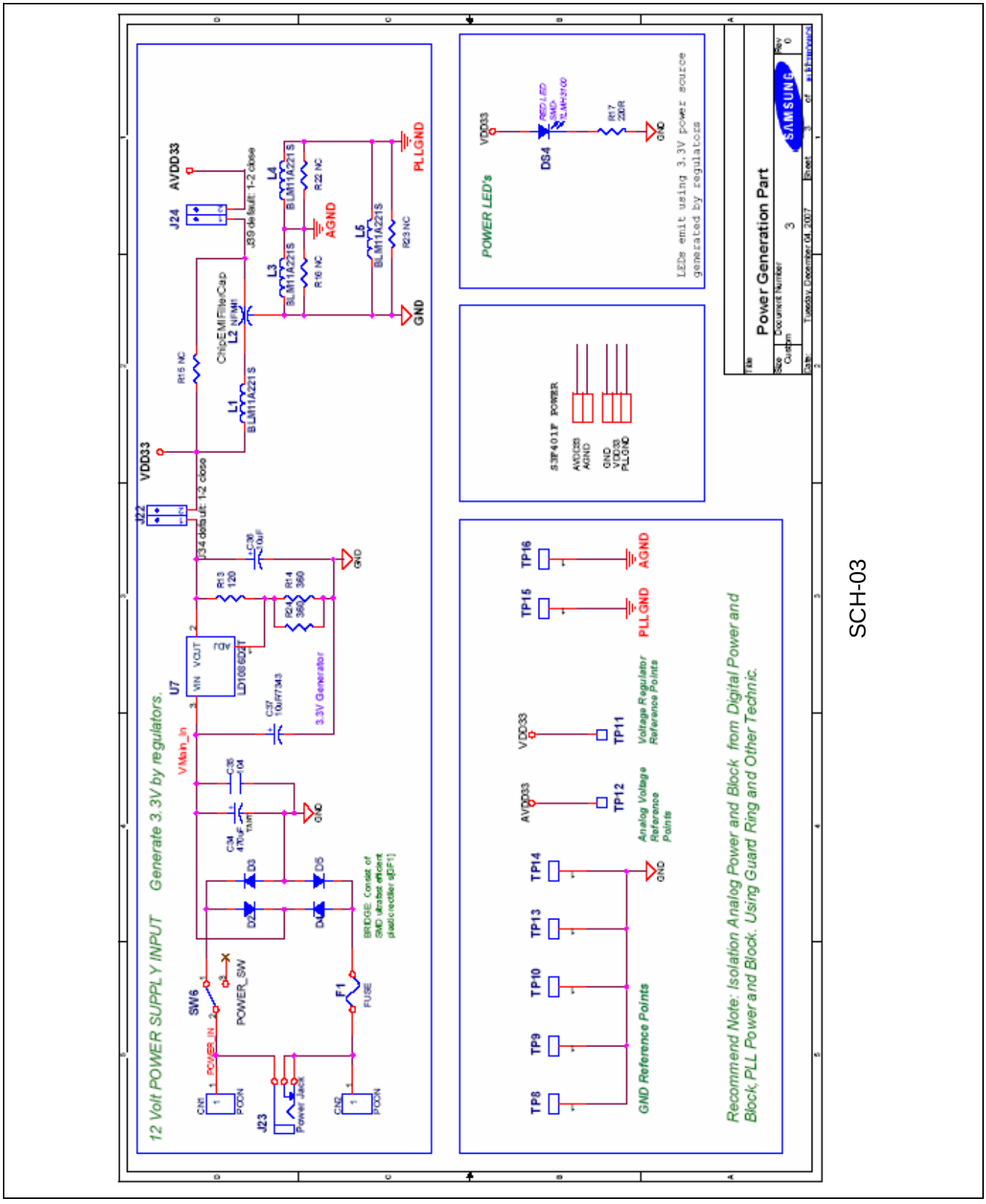
SW#	Description	
SW1	7-Segment	ON: Port 0.0~0.7 connects to 7segment
SW2	Latch	ON: Port 1.9~1.12 connects to latch
SW3	INT7	LOW signal is generated by SW3
SW4	INT8	HIGH signal is generated by SW4
SW5	RESET	Reset signal is generated by SW6
SW6	Power_VIN	Power on switch
SW7	SSP16	Port connects to EEPROM
SW8	SSP16	Port connects to EEPROM
SW9	SSP8	Port connects to EEPROM
SW10	SSP8	Port connects to EEPROM
SW11	AIN	Port connects to ADC
SW12	AIN	Port connects to ADC

4. S3F401F-EVB REV 1.0 BOARD SCHEMATICS

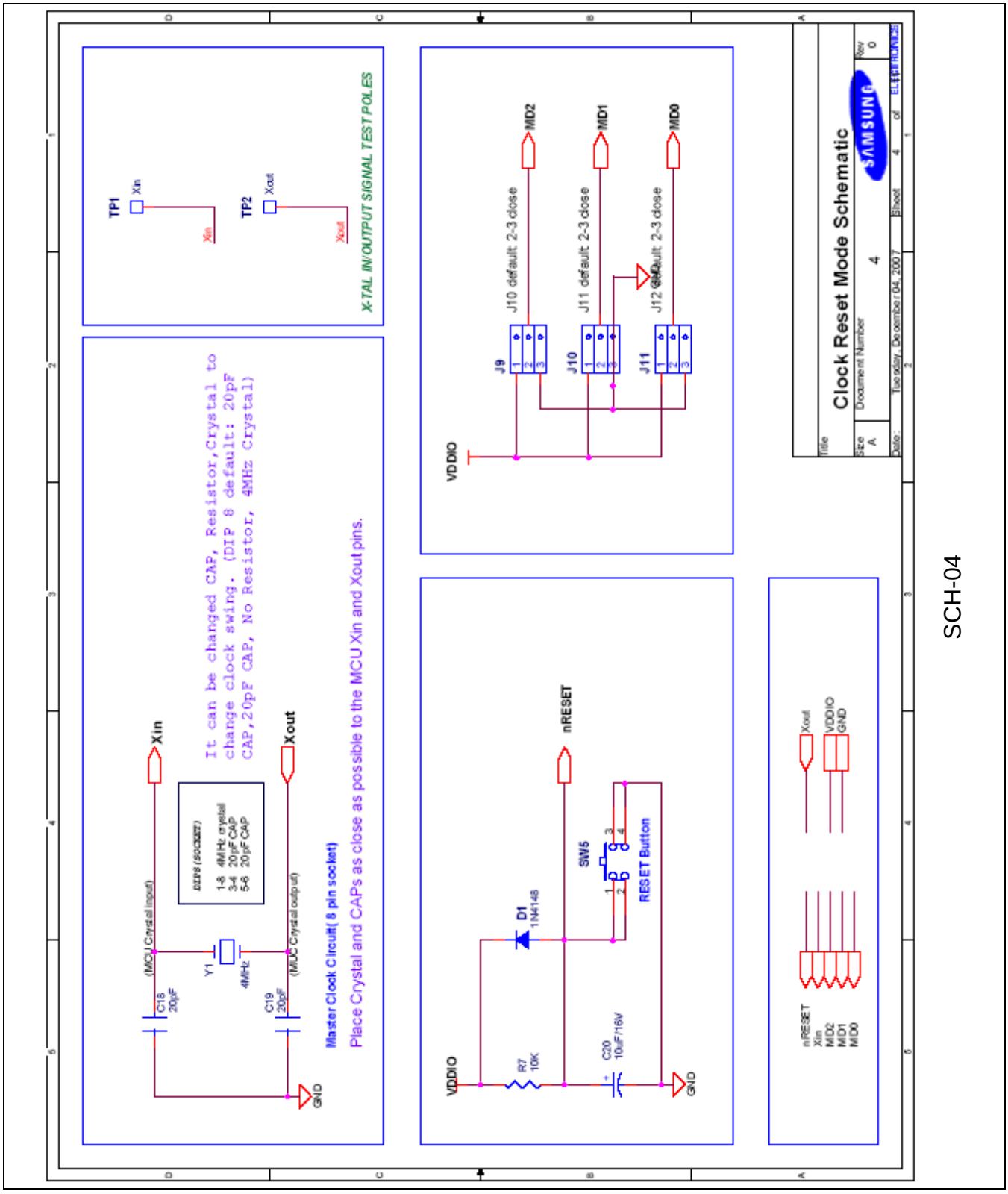
SCH-01	EVB TOP Block Diagram	REV 1.0
SCH-02	S3F401F Micro-Controller	REV 1.0
SCH-03	System Power Generation	REV 1.0
SCH-04	Clock & Mode	REV 1.0
SCH-05	ADC, Interrupt & BUZZER	REV 1.0
SCH-06	JTAG Connector	REV 1.0
SCH-07	UART Communication	REV 1.0
SCH-08	SSP Communication	REV 1.0
SCH-09	IMC & ENC Signal	REV 1.0
SCH-10	7-Segment Display	REV 1.0
SCH-11	Expansion Connector	REV 1.0


S3F401F Evaluation Board Top Block
S3F401F
SCH-01

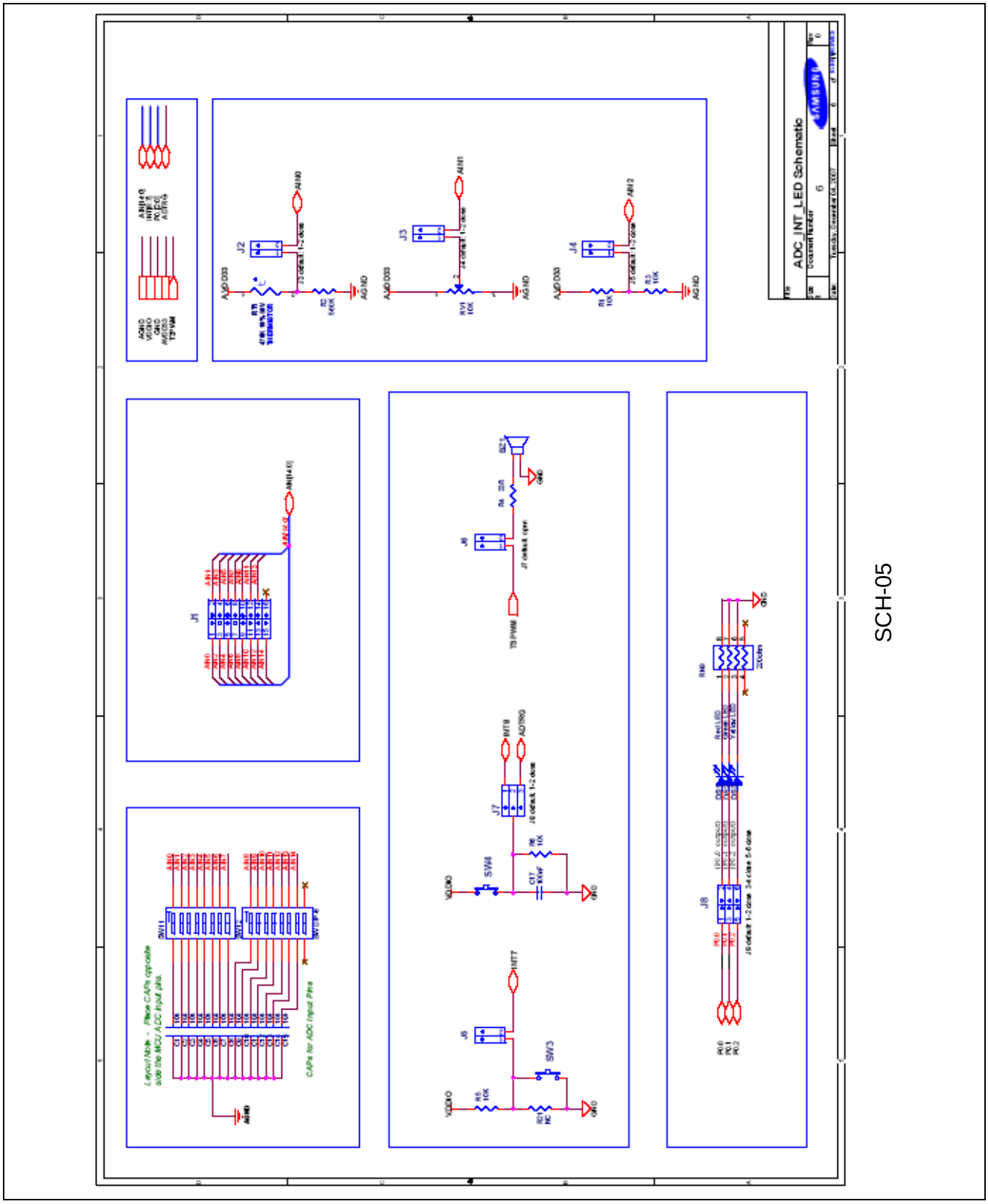

S3F401F
Pins for S3F401F's Supply Power
Power Voltage Monitoring Points
Layout Note - Place Power CAPs as close as possible to each pin of MCU.
SCH-02

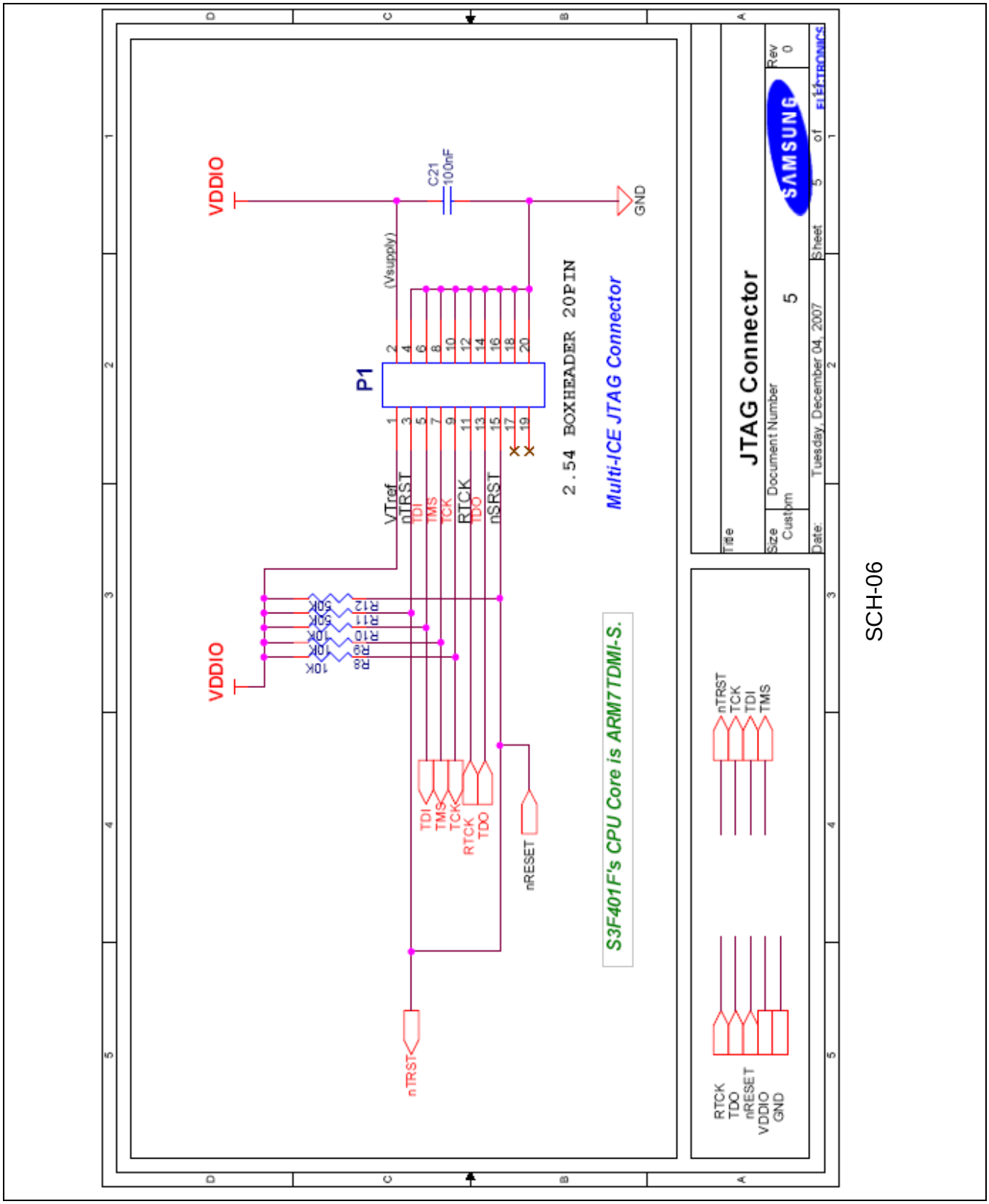

12 Volt POWER SUPPLY INPUT Generate 3.3V by regulators.
3.3V Generator
POWER LED's
S3F401F POWER
Power Generation Part
Recommend Note: Isolation Analog Power and Block from Digital Power and Block,PLL Power and Block. Using Guard Ring and Other Technic.
GND Reference Points
Analog Voltage Reference Points
Voltage Regulator Reference Points
LEDs emit using 3.3V power source generated by regulators
SAMSUNG

SCH-03

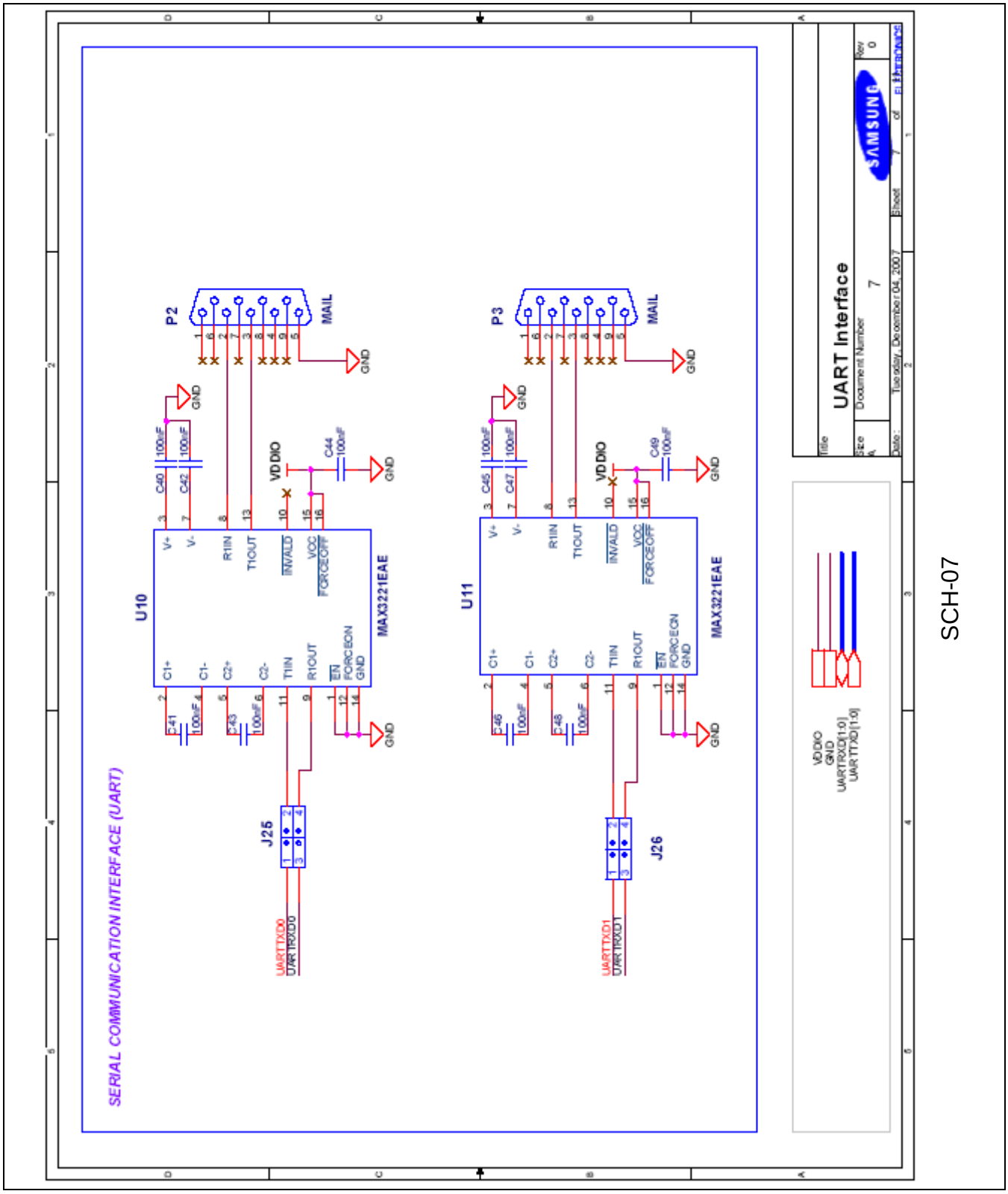

TP1
Xin
TP2
Xout
X-TAL IN/OUTPUT SIGNAL TEST POLES
It can be changed CAP, Resistor,Crystal to change clock swing. (DIP 8 default: 20pF CAP,20pF CAP, No Resistor, 4MHz Crystal)
Xin
Xout
(MCU Crystal input)
(MUC Crystal output)
C18 20pF
Y1 4MHz
C19 20pF
GND
Master Clock Circuit(8 pin socket)
Place Crystal and CAPs as close as possible to the MCU Xin and Xout pins.
J9
J10
J11
J10 default: 2-3 close
J11 default: 2-3 close
MD2
MD1
MD0
VDDIO
nRESET
D1 1N4148
SW5
RESET Button
R7 10K
C20 10uF/16V
Clock Reset Mode Schematic
SAMSUNG
Document Number
4
Tuesday, December 04, 2007
nRESET
Xin
MD2
MD1
MD0
Xout
VDDIO
GND

SCH-04

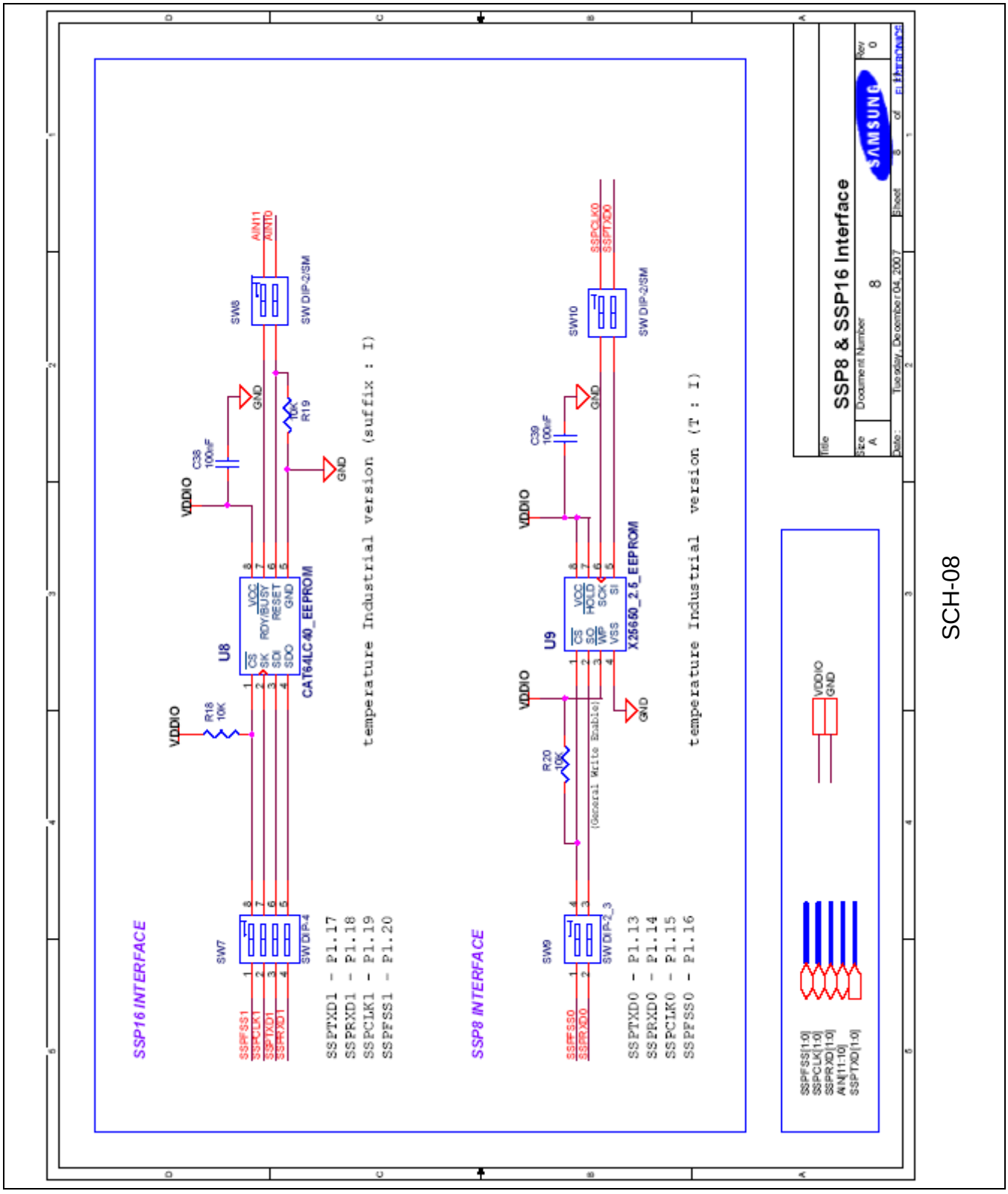

ADC_INT_LED Schematic
SCH-05


VDDIO
C21
100nF
GND
(Vsupply)
P1
2.54 BOXHEADER 20PIN
Multi-ICE JTAG Connector
VTref
nTRST
TDI
TMS
TCK
RTCK
TDO
nSRST
R12 50K
R11 50K
R10 10K
R9 10K
R8 10K
VDDIO
S3F401F's CPU Core is ARM7TDMI-S.
nRESET
JTAG Connector
Size Custom
Document Number 5
Rev 0
Date: Tuesday, December 04, 2007
Sheet 5 of 1
nTRST
TCK
TDI
TMS
RTCK
TDO
nRESET
VDDIO
GND

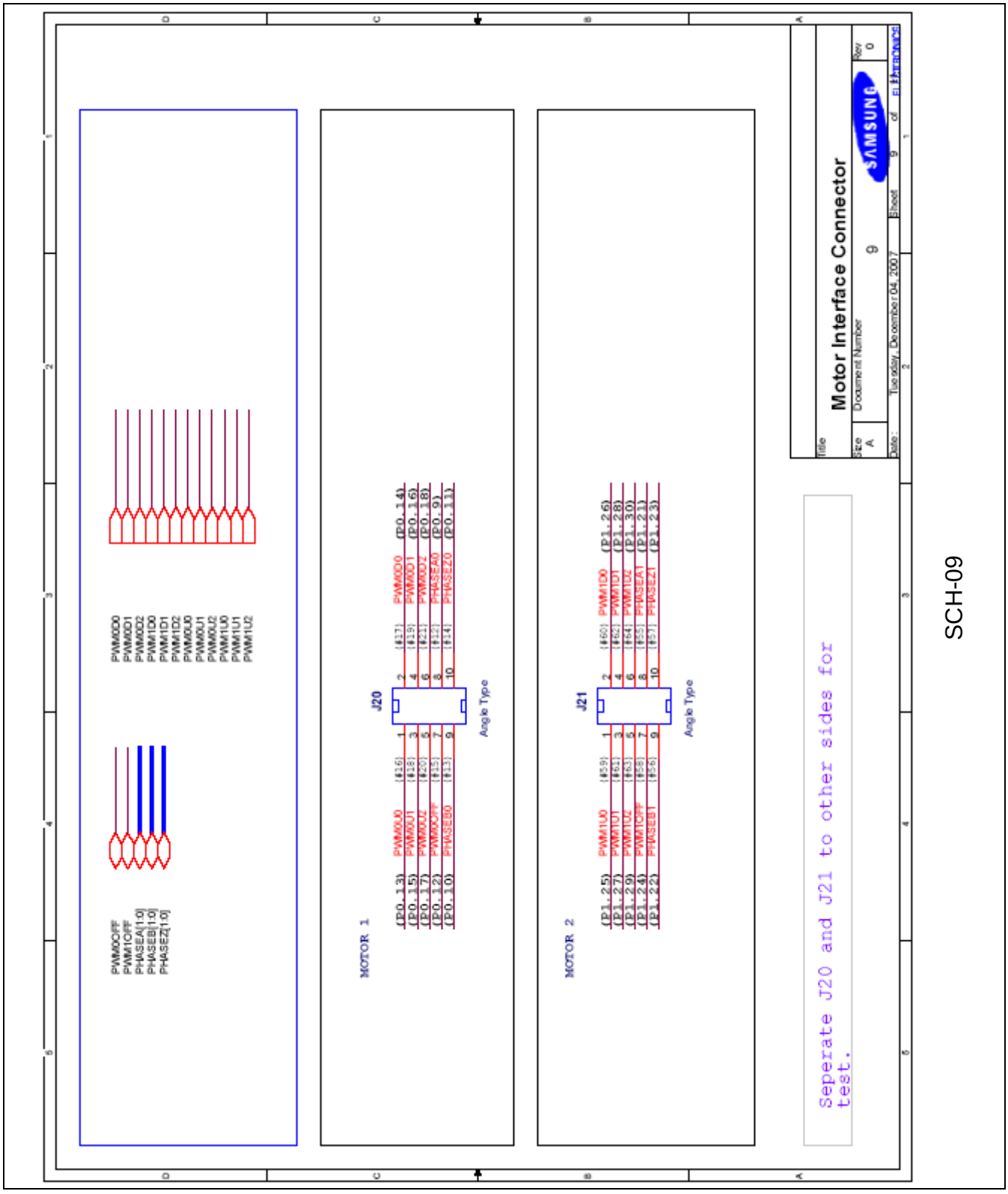
SCH-06


SERIAL COMMUNICATION INTERFACE (UART)
P2
P3
MAIL
GND
VDDIO
U10
U11
MAX3221EAE
J25
J26
UART Interface
SAMSUNG
VDDIO
GND
UARTRXD[1:0]
UARTTXD[1:0]

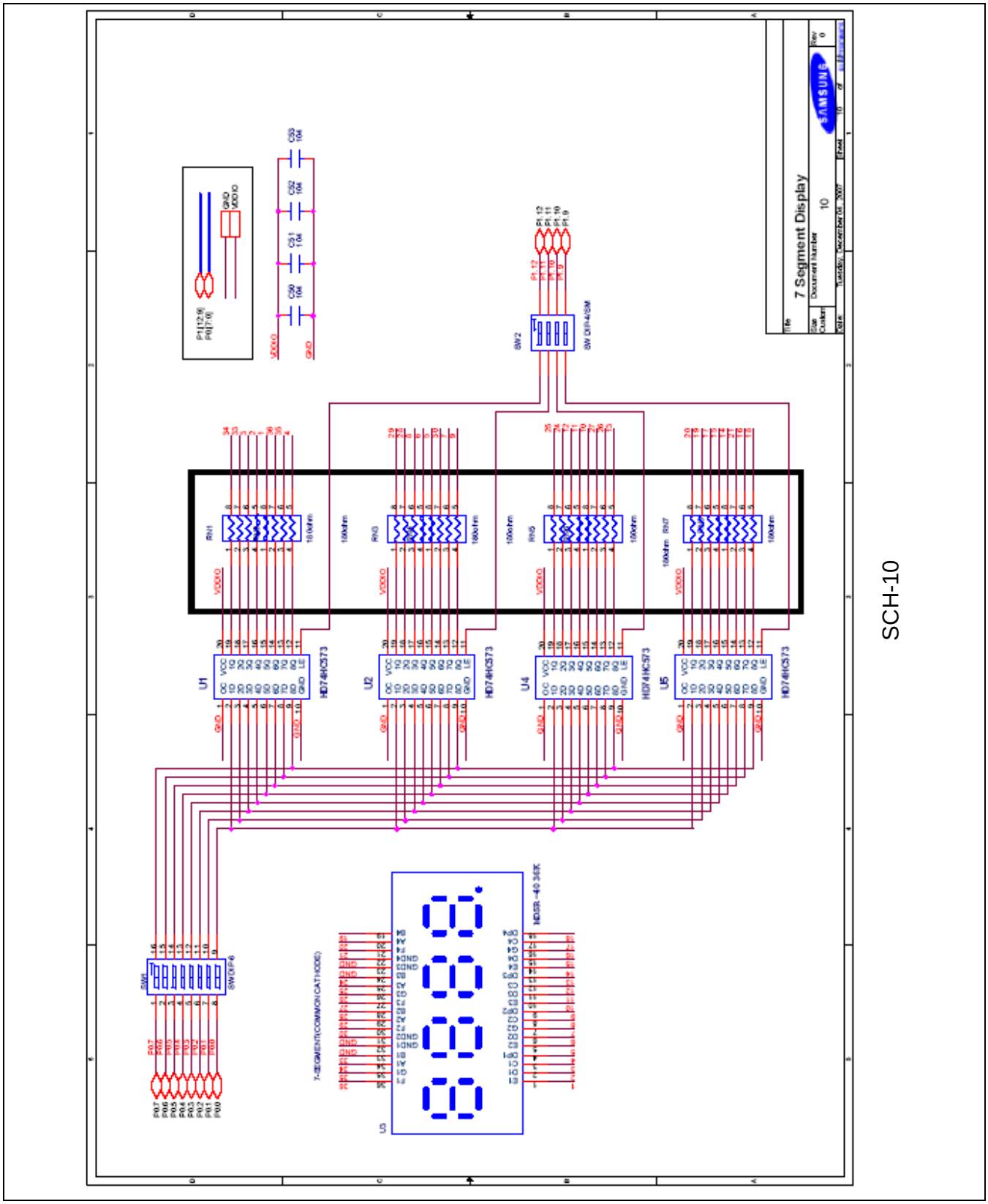
SCH-07

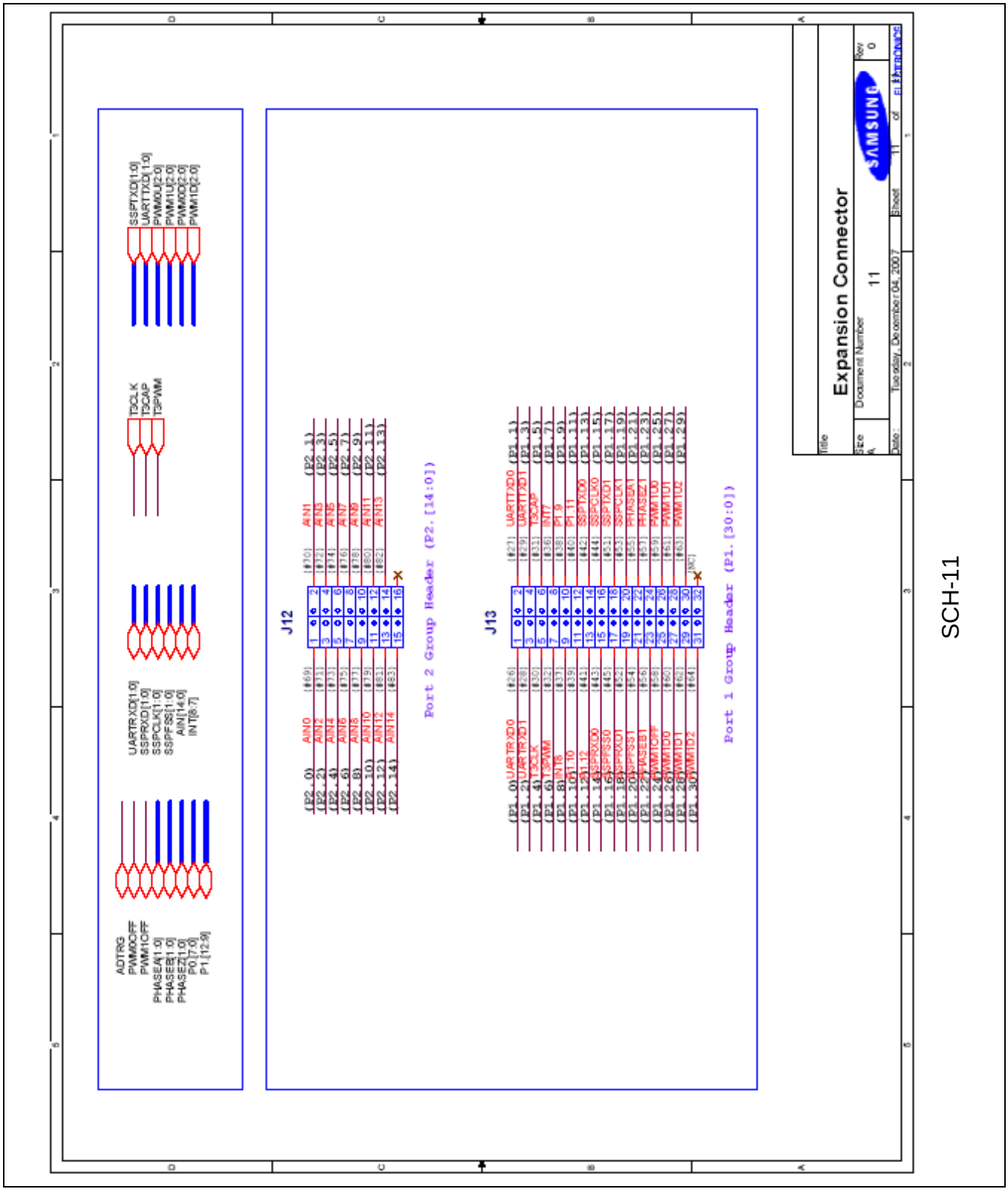

SSP16 INTERFACE
SSP8 INTERFACE
SSP8 & SSP16 Interface
SAMSUNG
SSPTXD1 - P1.17
SSPRXD1 - P1.18
SSPCLK1 - P1.19
SSPFSS1 - P1.20
SSPTXD0 - P1.13
SSPRXD0 - P1.14
SSPCLK0 - P1.15
SSPFSS0 - P1.16
temperature Industrial version (suffix : I)
temperature Industrial version (T : I)
CAT64LC40_EEPROM
X25660_2.5_EEPROM
SW DIP-4
SW DIP-2/SM
SW DIP-2_3
VDDIO
GND
U8
U9
SW7
SW8
SW9
SW10
R18 10K
R19 10K
R20 10K
C38 100nF
C39 100nF
AIN11
AIN10
SSPCLK0
SSPTXD0
SSPFSS1
SSPCLK1
SSPTXD1
SSPRXD1
SSPFSS0
SSPRXD0
(General Write Enable)
SSPFSS[1:0]
SSPCLK[1:0]
SSPRXD[1:0]
AIN[11:10]
SSPTXD[1:0]

SCH-08


Motor Interface Connector
Size A
Document Number
9
Rev 0
Sheet 9 of 9
Date: Tuesday, December 04, 2007
SAMSUNG ELECTRONICS
PWM00D0
PWM00D1
PWM00D2
PWM1D0
PWM1D1
PWM1D2
PWM00U0
PWM00U1
PWM00U2
PWM1U0
PWM1U1
PWM1U2
PWM00OFF
PWM1OFF
PHASEA[1:0]
PHASEB[1:0]
PHASEZ[1:0]
J20
MOTOR 1
Angle Type
J21
MOTOR 2
Angle Type
Seperate J20 and J21 to other sides for test.

SCH-09


7 Segment Display
SAMSUNG
U1
U2
U4
U5
HD74HC573
SW1
SW2
SCH-10


Expansion Connector
Port 2 Group Header (P2.[14:0])
Port 1 Group Header (P1.[30:0])
J12
J13
SSPTXD[1:0]
UARTTXD[1:0]
PWM0UE[2:0]
PWM1UE[2:0]
PWM0OE[2:0]
PWM1OE[2:0]
T0CLK
T0CAP
T0PWM
UARTRXD[1:0]
SSPRXD[1:0]
SSPCLK[1:0]
SSPFSS[1:0]
AIN[14:0]
INT[6:7]
ADTRG
PWM0OFF
PWM1OFF
PHASEA[1:0]
PHASEB[1:0]
PHASEZ[1:0]
P0[7:0]
P1[12:9]

SCH-11